REMARKS:

Claims 10 and 13-15 are currently being considered, of which claim 10 has been amended herein and claim 15 has been newly added herein. Claims 11 and 12 have been canceled without prejudice or disclaimer as to their subject matter. Applicant respectfully believes that no new matter has been introduced.

A. Informalities:

The Examiner has objected to claims 10-14 because of various noted informalities. Claim 10, as amended, includes --a memory area-- (line 9) and --one over an integer -- (line 14). Thus, Applicant respectfully submits that this objection should be withdrawn.

B. Present Invention:

Before turning to the cited art, a review of the present invention is in order. According to the present invention, a first image signal of a first resolution which corresponds to an optical image of an object scene is output from an imaging device at a rate of one screen per a first period. A creator creates a second image signal of a second resolution lower than the first resolution by subjecting the first image signal to a signal processing including a thinning-out process. The second image signal is also created at a rate of one screen per the first period.

A writer writes the second image signal created by the creator to a memory having a single input/output port. More specifically, the second image signal created by the creator is first held by a buffer, and then transferred from the buffer to the memory by a transferor. Herein, an SDRAM is adopted as the memory. The second image signal is thus written to the memory at a rate of one screen per the first period. The second image signal stored in the memory is read out by a reader at a rate of one screen per a second period which is shorter than the first period. A displayer displays an image based on the read second image signal.

Thus, the creator creates the second image signal at a rate of one screen per the first period, while the displayer displays the image based on the second image signal at a rate of one screen per the second period. That is, a screen rate is different between the creator and the displayer. Thereupon, if the second image signal created by the creator is directly applied to the displayer, a process is broken down.

This is the reason why the memory is provided between the creator and displayer in the present invention. The second image signal created at a rate of one screen per the first period is written to the memory, and thereafter read out from the memory at a rate of one screen per the second period. The difference of the screen rate is absorbed by such a memory access operation, and therefore, the process is prevented from being broken down because of the difference of the screen rate.

However, since the second period is shorter than the first period, the second image signal of an amount exceeding one screen is read out from the memory during the second image signal of one screen being written to the memory. This operation signifies that the more the second period is short, the more the amount of memory access is increased. Thereupon, regarding a memory which inputs/outputs data using a single port, a process is broken down unless an access speed is increased.

This is the reason why the SDRAM is adopted as the memory. A burst transfer is available for the SDRAM, and therefore, it is possible to increase the access speed.

However, the burst transfer is of accessing sequential column addresses belong to a designated row address, and the more the amount of data transfer at one time is large, the more the access speed is increased. In other words, when the amount of data transfer at one time is small, the access speed is decreased because of an overhead.

This is the reason why the second image signal created by the creator is first held by the buffer, and then transferred to the SDRAM in the present invention. An intermittent pixel arrangement of the second image signal caused by the thinning-out process is converted to a sequential pixel arrangement in the buffer. This makes it possible to use an advantage of the burst transfer, and therefore, the access speed is increased.

That is, according to the present invention, a break down of the process caused by the difference of the screen rate between the second image signal created by the creator and the second image signal being subjected to a display process is prevented by providing the memory between the creator and the displayer, and a break down of the process caused by slowness of a memory access speed is prevented by adopting the SDRAM as the memory and temporarily holding the second image signal from the creator in the buffer.

C. 35 USC 103(a):

Claims 10-14 stand rejected under 35 U.S.C. 103(a) as obvious over USP 5,734,427 (**Hayashi**) in view of USP 6,295,596 (**Hirabayashi**) and USP 5,835,164 (**Kanai**).

Applicant respectfully traverses this rejection.

1. Hayashi:

Hayashi discloses to convert pixel data of horizontal 1280 x vertical 1024 dots based on an output of a CCD to pixel data of horizontal 640 x vertical 512 dots by a thinning-out process so as to output the converted pixel data to a monitor via a first memory and a second memory each of which has a capacity corresponding to horizontal 640 x vertical 512 dots.

However, according to the disclosure of **Hayashi**, frame rates of the CCD and the monitor coincide with each other, and either the first memory or the second memory is a dual-port memory. Accordingly, no break down occurs because of a difference of the frame rate or slowness of a memory access speed.

Consequently, **Hayashi** fails to describe, teach, or suggest anything about a constitution of the present invention in which the second image signal output from the buffer is written in the SDRAM having a single input/output port. Accordingly, Applicant believes that it would not be possible for one of ordinary skill in the art to arrive at the present claimed invention based on the teachings of **Hayashi**. **Hayashi** fails to describe, teach, or suggest the digital camera, imaging device, creator, first and second image signals, memory, single input/output port, SDRAM, buffer, and transferor as set forth in claim 10, as amended.

2. <u>Hirabayashi</u>:

Hirabayashi discloses to write data while switching banks for each row of the PI or PO series such that the data can be read out fast with a long burst length in one series, while the data can be read out fast by bank switching in another series.

However, according to **Hirabayashi**, neither data from a disk is subject to a thinning-out process, nor thinned data is stored in a buffer prior to writing in an SDRAM. That is, **Hirabayashi** fails to describe, teach, or suggest anything about a constitution of the present invention in which the second image signal obtained by the thinning-out process is written in the SDRAM via the buffer. Accordingly, Applicant believes that it would not be possible for one of ordinary skill in the art to arrive at the present claimed invention based on the teachings of **Hirabayashi**. **Hirabayashi** fails to describe, teach, or suggest the digital camera, imaging device, creator, first and second image signals, memory, single input/output port, SDRAM, buffer, and transferor as set forth in claim 10, as amended.

3. **Kanai**:

Kanai discloses to write data into a memory at a first rate based on a writing control clock and read the data from the memory at a second rate which is n times the first rate (n is an integer greater than one).

However, the memory adopted by **Kanai** is a dual-port memory similar to that of **Hayashi**. With regard to a dual-port memory, no written data clashes with read data, and therefore, there is no need to provide a buffer for temporarily holding the written data at a previous step of the dual-port memory.

Consequently, **Kanai** also fails to describe, teach, or suggest anything about a constitution of the present invention in which the second image signal to be written to the SDRAM is temporarily held in the buffer. Accordingly, Applicant believes it would not be possible for one of ordinary skill in the art to arrive at the present claimed invention based on the teachings of **Kanai**. **Kanai** fails to describe, teach, or suggest the digital camera, imaging device, creator, first and second image signals, memory, single input/output port, SDRAM, buffer, and transferor as set forth in claim 10, as amended.

4. <u>Combination of Hayashi, Hirabayashi, and Kanai</u>:

Hayashi, **Hirabayashi**, and **Kanai**, alone or in combination, fail to describe, teach, or suggest the present claimed invention.

In case the first memory or the second memory disclosed by **Hayashi** as a dual-port memory is replaced with the SDRAM having a single port disclosed by **Hirabayashi**, a process is broken down unless a buffer for temporarily holding data to be written to the SDRAM is provided. That is, the buffer must be inserted between the SDRAM and each of an R adder, a G adder and a B adder. Since such a buffer is not disclosed in **Hayashi**, Applicant believes that it would not be possible for one of ordinary skill in the art to arrive at the present claimed invention based on the teachings of a combination of **Hirabayashi** with **Hayashi**.

Consequently, Applicant believes that even if it were possible to combine **Kanai**, which discloses a memory reading speed being higher than a memory writing speed, with **Hayashi**, it would not be possible for one of ordinary skill in the art to arrive at the present claimed invention based on the teachings of such a combination, and therefore, the rejection should be withdrawn.

Hayashi, Hirabayashi, and **Kanai**, alone or in combination, fail to describe, teach or suggest the following features set forth in claim 10, as amended: "A digital camera, comprising:
an imaging device for outputting, at a rate of one screen per a first period, a first image signal of a first resolution which corresponds to an optical image of an object scene; a creator for creating a second image signal of a second resolution lower than the first resolution by subjecting the first image signal outputted from said imaging device to a signal processing including a thinning-out process; a memory having a single input/output port and a plurality of memory areas; ... wherein said memory is an SDRAM, and said writer includes a buffer for holding the second image signal created by said creator, and a transferor for transferring the second image signal held by said buffer to said memory", in combination with the other claimed features.

Thus, Applicant respectfully submits that the rejection should be withdrawn.

D. Claim 15:

Claims 15 has been newly added. Applicant has presented this additional claim to alternatively and more completely define Applicant's invention and thereby assist the Examiner by facilitating the speedy and compact prosecution of the present application.

Although the Office Action mailed August 3, 2004 did not address this claim 15, not hitherto available to the Examiner, Applicant desires to make a record as to why the cited art does not make it obvious, and desires to otherwise indicate why it is patentable.

Hayashi, Hirabayashi, and Kanai, alone or in combination, fail to describe, teach, or suggest the following features as set forth in claim 15: the imaging device, creator, memory, writer, reader, and displayer, "wherein said memory is an SDRAM, and said writer includes a buffer for holding the second image signal held by said buffer to said memory", in combination with the other claimed features.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

Darren R. Crew

Darren R. Crew
Attorney for Applicant
Reg. No. 37,806

DRC/llf
Atty. Docket No. **991142**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE